Patent claims

1. A method for fabricating a diode (DL) of small dimensions between two silicon electrodes (ELn, GRST) deposited above a substrate (30), which comprises the following steps:

- a) producing the two electrodes, separated by a gap, above the substrate,
- b) thermally oxidizing a part of the thickness of the electrodes, in height and in width, leaving a space remaining between the oxidized electrodes, the substrate being protected against oxidation in this space;
- c) exposing the surface of the substrate in this space,
- d) depositing a layer of doped polycrystalline silicon (40) entering in contact with the substrate in this space in order to form one pole (42) of the diode, the substrate forming the other pole,
- e) partially removing the polycrystalline silicon while leaving a desired pattern remaining, this pattern covering at least the space left between the electrodes and also covering a region lying outside this space,
- f) depositing an insulating layer (18), locally etching an opening (50) into this insulating layer above the polycrystalline silicon outside the space lying between the electrodes, in order to form an offset contact zone, depositing a metal layer (22) entering in contact with the polycrystalline silicon in the offset contact zone, and etching the metal layer according to a desired pattern of interconnections.

2. The method as claimed in claim 1, characterized in that for step e) of partially removing the polycrystalline silicon, a uniform layer of silicon nitride (46) is deposited, this is etched according to a pattern which leaves the layer remaining above the polycrystalline silicon zones that are intended to be

kept, and the silicon is subsequently oxidized over its entire thickness wherever it is not covered with nitride, until a silicon pattern is obtained which comprises only the zones that were not covered with nitride.

3. The method as claimed in claim 2, characterized in that between the deposition of the nitride layer and the subsequent step of oxidizing the polycrystalline silicon, the polycrystalline silicon is chemically attacked in order to remove it as much as possible wherever it is not protected by the nitride.

4. An integrated circuit comprising a CCD register with a readout diode at the end of the register, between the last electrode of the register and a reset electrode, characterized in that the readout diode consists of a doped region (42) delimited on one side by the electrodes and on the other side by regions of thick silicon oxide (10), the doped region being entirely covered with a layer of polycrystalline silicon (14, 40) delimited according to a pattern which extends partly above the thick oxide, the silicon layer being covered with an insulating layer (18) comprising an opening (50) above the thick oxide but no opening above the doped region, and the insulating layer being itself covered with a conductive layer entering in contact with the polycrystalline silicon through the opening (50).

5. The integrated circuit as claimed in claim 4, characterized in that the polycrystalline silicon layer is covered with silicon nitride, itself covered by the insulating layer (50), the nitride layer also being open at the position of the opening in the insulating layer.